S1022/8056 **VOLTAGE REFERENCE IN AN INTEGRATED CIRCUIT** 177656

Background Of The Invention

1. Field of the Invention

The present invention relates to the field of integrated circuits and more specifically to the formation of a voltage reference in an integrated circuit.

2. Discussion of the Related Art

A voltage reference is a device which exhibits a substantially constant voltage thereacross when it conducts a current located in a given range of values.

A desired feature for a voltage reference first is that the voltage thereacross remains as constant as possible when the current which flows through the voltage source varies over a relatively wide range.

Another desired feature is that this voltage is stable over time and temperature.

A first conventional type of voltage reference is a so-called band-gap voltage reference which forms a particularly accurate and stable voltage reference but which uses a great number of components and which occupies a non-negligible integrated circuit surface. Thus, such voltage sources are not adapted, in particular, to forming protection devices to limit to a determined voltage the voltage between two terminals of a device to be protected, for example between the gate and the source of a MOS transistor.

Another known voltage reference is the zener diode. This voltage reference has the advantage of being relatively simple to implement in an integrated circuit and to occupy a small surface therein. A zener diode may simply be used as a voltage source or as a protection device at a given voltage. However, this device has the disadvantage of being unstable over time, that is, if its nominal current is circulated through a zener diode for a long time, the voltage thereacross drifts. For example, for a conventional zener diode made at the surface of an integrated circuit, the nominal voltage variation is currently on the order of 0.06 volt per hour and can reach a value on the order of one volt after 1000 hours of use. Further, an integrated circuit zener diode has a constant voltage only over a small current range.

Summary Of The Invention

Thus, an object of the present invention is to provide a voltage reference implementable in an integrated circuit and having the simplicity of a zener diode and its low surface area requirement,

but the voltage of which is constant over a wider current range.

Another objet of the present invention is to provide a voltage reference which is stable over time.

Another object of the present invention is to provide a voltage reference which is implementable as simply in a bipolar integrated circuit as in a MOS-type integrated circuit.

To achieve these and other objects, the present invention provides a voltage reference in an integrated circuit, formed of an NPN bipolar transistor, the base of which is not connected and the emitter of which corresponds to an anode, and the collector of which corresponds to a cathode.

According to an embodiment of the present invention, the transistor is an NPN bipolar transistor of a bipolar-type integrated circuit.

According to an embodiment of the present invention, the NPN bipolar transistor is formed in an N well of a MOS-type integrated circuit, the emitter corresponding to a drain-source region of an N-channel MOS transistor formed in a region corresponding to a drain-source region of a P-channel MOS transistor.

The foregoing objects, features and advantages of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

Brief Description Of The Drawings

Fig. 1 shows the equivalent diagram of a voltage reference according to the present invention;

Fig. 2 shows a voltage reference according to the present invention formed of an NPN-type bipolar transistor in a bipolar-type integrated circuit;

Fig. 3 shows a voltage reference according to the present invention formed of an NPN-type bipolar transistor in a MOS-type integrated circuit;

Fig. 4 shows the current-voltage characteristic of a voltage reference according to the present invention and, as a comparison, the current-voltage characteristic of a usual integrated circuit zener diode, the current being in logarithmic scale;

Fig. 5 shows the current-voltage characteristic of a voltage reference according to the present invention, the current being in linear scale; and

Fig. 6 very schematically shows the characteristic of voltage variation over time of a voltage source according to the present invention compared with a zener diode.

As is schematically shown in Fig. 1, the present invention uses, as a two-terminal device, an NPN-type bipolar transistor connected between its collector and its emitter, its base being unconnected (maintained floating). Emitter terminal E corresponds to the anode terminal (+) and collector terminal C corresponds to the cathode terminal (-) of the dipole. It will be shown hereafter that such a device can be used in the same way as a zener diode but has the advantage of better stability over time and of a smaller voltage dispersion over a wide current range.

Fig. 2 shows a first embodiment of the present invention. This drawing shows a conventional NPN transistor formed in a bipolar integrated circuit. The bipolar transistor corresponds to a conventional technology in which a lightly-doped N-type epitaxial layer 1 is formed on a P-type silicon substrate 2. At the transistor location a buried layer 3 is formed, before the growth of the epitaxial layer. The bipolar transistor includes a P-type base region 5 formed in the epitaxial layer, an N-type emitter region 6 formed in base region 5 and an N^+-type region 7 used as a collector contact. Preferably, this region extends in a collector well to contact buried layer 3. Preferably, to ensure its isolation, the component is surrounded with a P-type isolating wall 8 which crosses epitaxial layer 1.

According to the present invention, this device is used as a voltage reference two-terminal device, that is, only an emitter metallization E is provided on emitter region 6 and a collector region C is provided on collector contacting area 7.

Fig. 3 shows an embodiment of the present invention implemented in a CMOS-type integrated circuit, that is, an integrated circuit in which it is provided to essentially form N-channel MOS transistors and P-channel MOS transistors. Consider, for example, in Fig. 3, a line in which a P-type epitaxial layer 11 is formed on a P^+-type substrate 12. In this technology, N-channel MOS transistors are formed directly in epitaxial layer 11 and P-channel MOS transistors are formed in N-type wells formed in this epitaxial layer. Reference 13 indicates an example of such a well in which a component according to the present invention is made. This component includes a P-type region 15 formed in well 13. This P-type region corresponds, for example, to the drain and source implantations-diffusions of the P-channel transistors. An N-type region 16 is formed in region 15. Region 16 corresponds, for example, to the drain and source implantations-diffusions of N-channel MOS transistors. Further, a collector contact recovery region 17 is formed at the same time as region 16. An NPN transistor, the emitter of which corresponds to region 16, the base of which corresponds to region 15, and the collector of which corresponds to region 17 is thus obtained. According to the

present invention, only an emitter metallization E and a collector metallization C are formed. The resulting NPN transistor will of course have a low gain since region 15 is relatively heavily-doped but is perfectly well adapted to the forming of a voltage reference according to the present invention.

The applicant has studied the current-voltage characteristic V_T of the two-terminal device of Figs. 1, 2, and 3. Figs. 4 and 5 show the characteristic of such a dipole in the specific case of Fig. 2. Figs. 4 and 5 show the same curve, the difference being that in Fig. 4, the current is plotted in logarithmic coordinates and that in Fig. 5, the current is plotted in linear coordinates.

More specifically, in an example of embodiment, the characteristics of the device of Fig. 2 are the following:

- for N^+-type region 6: junction depth x_j = 0.25 μm, surface concentration C_s = 1 to 3.10^{20} at./cm^3, sheet resistance = 20 to 50 ohms;

- for P-type region 5, junction depth x_j = 0.4 to 0.5 μm, concentration at the junction with region 6 C_{xj} = 2 to 7.10^{17} at./cm^3, sheet resistance = 600 to 1000 ohms, sheet resistance under region 6 = 5 to 12 kohms.

Voltage V_T appears to grow substantially regularly with the current until it reaches a threshold value, equal to 4.74 volts in the example shown, while the current remains lower than 1 microampere. Then, the voltage between terminals E and C remains substantially constant while the current increases from a value on the order of 1 μA to a value on the order of 10 mA. More specifically, a voltage of 4.80 volts has been measured for 11.6 mA. Eventually, for higher current values, the voltage varies according to the impedance of the circuit in which the component according to the present invention is inserted.

A very small voltage dispersion (on the order of 1 %) should thus be noted for current values increasing in a ratio of 1 to 10,000. A particularly stable voltage source, independent from the current flowing therethrough, has thus been obtained.

Similar results may be observed whatever structure is used, especially in the case of a structure of the type of that in Fig. 3. It should besides be noted that these structures are likely to have a great number of alternatives, and can thus be implemented in a great number of technological lines, for example, in the case of Fig. 3, the present invention also is operative when epitaxial layer 11 is formed on an N-type substrate. It also is operative whether a buried layer is provided or not and, as indicated previously, whether a collector well is provided or not. The advantage of the provision of

the collector well and of the buried layer is that the dynamic operating range is increased.

Fig. 4 also shows as a comparison the characteristic of an equivalent zener diode formed of a region of a first type of conductivity formed in the region of the opposite type of conductivity at the surface of an integrated circuit.

It should be noted that the stabilization area of the zener diode is lower than three decades (from 1 μA to less than 1 mA) and that, over this area, the voltage varies by approximately 0.25 V. The voltage dispersion thus is on the order of 5 %, that is, much higher than with the present invention and over a smaller range.

Further, Fig. 6 shows the voltage variation over time. With a device according to the present invention, this variation is very low, for example, over a duration of 5000 seconds, for a nominal voltage on the order of 5 volts, a voltage variation lower than the accuracy of the measuring device which is 5 mV has been observed whereas, with a zener diode, the characteristic VZ has a variation of substantially 50 mV after 5000 seconds of operation. Further, if the operation of the zener diode is pursued during, for example, one thousand hours, a voltage variation on the order of one volt may be observed.

Thus, the device according to the present invention reaches the desired objects of providing a voltage reference which is stable over a wide current range and of providing a voltage which is stable over time. Further, the temperature stability is at least equal to that of a zener diode (on the order of + 1 mV/°C).

The present invention is particularly well adapted to the implementation of voltage references in integrated circuits of very small dimensions, for example submicronic.

Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is: